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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Gregory D Caldwell
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard 7th Floor
Los Angeles, CA 90025

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,812	SHOEMAKER, KEN	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 9-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Simultaneous Multithreading: A Platform for Next-Generation Processors, Susan Eggers, et al. (hereinafter referred to as Eggers et al.).

3. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on June 23, 2004.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simultaneous Multithreading: A Platform for Next-Generation Processors, Susan Eggers, et al. (hereinafter referred to as Eggers et al.).

6. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on June 23, 2004.

Response to Arguments

7. Applicant's arguments filed October 15, 2004 have been fully considered but they are not persuasive.

8. On page 7, Applicant argues in essence:

"Eggers discloses only a single instruction fetch unit that separately fetches two instructions. The office action relies on Page 14, left hand column of Eggers for allegedly describing that the single fetch unit "partitions itself among the threads." However, Applicants are unable to identify any teaching of such "partitioning." If the rejection is maintained applicants respectfully request clarification of the precise portion of Eggers which allegedly describes such partitioning, justifying the Examiner's reliance on a single fetch unit for anticipating the recited first and second fetch units."

Applicant is directed to page 14, specifically the left hand column, lines 38-48 (See the newly provided marked up copy of the reference.). Eggers et al. have specifically taught "an SMT fetch unit can take advantage of the interthread competition for instruction bandwidth to enhance performance. First it [the fetch unit] can partition this bandwidth among the threads. This is an advantage, because branch instructions and cache-line boundaries often make it difficult to fill issue slots if the fetch unit can access only one thread at a time. We fetch from two threads each cycle to increase the probability of fetching only useful (nonspeculative) instructions. In addition, the fetch unit can be smart about which thread it fetches, fetching those that will provide the most immediate performance benefit." Therefore this argument is moot.

9. On page 8, Applicant argues in essence:

"However, the cited portion merely generally describes how one form of SMT might work, and does not describe a scheduler unit coupled to a first and second instruction fetch units. In fact, the entire reference is devoid of any block diagram or other structural description of a fully functional SMT processor."

However, in this case it is not necessary for the Eggers et al. reference to have a specific block diagram or other structural description of a fully functional SMT processor for Eggers et al. to read on the claims. Claim 1 merely requires a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit. Any coupling, including direct or indirect meets the claimed invention. The first and second instruction fetch units, and the scheduler unit, as taught by Eggers et al. are described as being a part of the SMT processor. Since the first and second instruction fetch units and the scheduler unit are all a part of the disclosed SMT processor, the units must inherently all be, either directly or indirectly, coupled to each other. Therefore this argument is moot.

10. On page 8, Applicant argues in essence:

"Claim 1 further recites an execution unit coupled to said scheduler unit ... Applicants have reviewed pages 13 and 14 and cannot identify any mention of an execution unit or how such unit might be interconnected with other units. Applicants are not required to guess as to how the reference is being applied to the claim. If the rejection is maintained, a new non-final action is respectfully requested with a sufficiently detailed explanation of the Examiner's position, so that a full and fair response may be made."

According to claim 1, the execution unit must be coupled to the scheduler unit. This coupling can be any kind of coupling, either a direct or indirect coupling. Furthermore, every processor has an execution unit that executes instructions. This execution is described on page 13, left hand column, lines 15, 25, 34, 51-52. The unit that performs the execution is an execution unit. This execution unit and the scheduler unit are all described as being a part of the SMT processor. Since the execution unit and the scheduler unit are all a part of the disclosed SMT processor, the units must inherently all be, either directly or indirectly, coupled to each other. Furthermore, the MPEP requires

that the second office action must be made final unless a new grounds of rejection is applied. Specifically the MPEP section 706.07 states:

> *"Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p)."*

In this case, the grounds of rejection have not been changed. As such, there is no basis in the MPEP for making this action Non-final. Therefore this argument is moot.

11. On pages 8-11, Applicant argues in essence:

"Claim 1 further recites a register file coupled to said execution unit, wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread. The office action relies on pages 14-15, particularly the section entitled "Register file and pipeline," for allegedly identically disclosing this claim recitation. Applicants are unable to identify any description in the cited portion that discloses a register file coupled to an execution unit or that the registers described in the "register file" section are used to switch either a first or second active thread with an inactive thread. ... Examiner's analysis with respect to how the fetching of instructions by Eggers' fetch unit teaches or suggest anything whatsoever in connection with the operation of Eggers' register file. The office action appears to be improperly conflating these two distinct components of Eggers in order to read on the claims. ...
With respect to claim 7, the office action again appears to improperly conflate the functions of Eggers' fetch unit with Eggers register file. The Examiner should unambiguously identify whether the rejection relies on Eggers' fetch unit or Eggers' register file for the recited switching, so that a full and fair response may be made."

However, Examiner is not conflating the register file with the fetch unit. In Eggers et al when the fetch unit switches one of said first active thread and said second active thread with a first inactive thread, the register files being accessed correspond to each particular thread being executed. So when two threads are being executed, the corresponding

register files for the two threads have been switched to and are being accessed. The register files effectively switch, along with the fetch unit, to one of said first active thread and said second active thread with a first inactive thread. Therefore the examiner has not conflated the fetch unit with the register file and this argument is moot.

12. On page 9, Applicant argues in essence:

"By way of background, some embodiments of the present invention may relate to multithreading processor which exhibits both simultaneous multithreading (SMT) capability and switch on event multithreading (SoEMT) capability. In contrast, Eggers describes only multithreading processors having either SMT or SoEMT capability."

Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

In this case, Applicant has not specifically claimed exhibiting both simultaneous multithreading (SMT) capability and switch on event multithreading (SoEMT) capability. Therefore this argument is moot.

13. On page 10, Applicant argues in essence:

"With respect to claim 2, applicants note that Eggers does not describe how the "hardware contexts for eight threads" are otherwise interconnected. In any event, they do not appear to be coupled to the disclosed "register file."

However, each element of the SMT processor is coupled, either directly or indirectly. In this case the on deck context unit (page 15, hardware contexts for eight threads) and the register file (pages 14 and 15, see the section entitled "Register file and pipeline") are all a part of the SMT processor and are therefore coupled. Therefore this argument is moot.

14. On page 10, Applicant argues in essence:

"With respect to claim 4, applicants note that the office action relies on page 14, first paragraph, which does not appear to mention any decoders. The only mention of decoding applicants can identify is in the paragraph spanning the left and right hand columns on Page 14, which describes that Eggers single fetch unit selects subset of instructions from two threads for decoding. Accordingly, Eggers does not teach or suggest first and second decode units. Accordingly, claim 4 is separately patentable over Eggers

...

With respect to claim 8, applicants again note that Eggers does not describe any particular structure for the SMT processor proposed therein. Moreover, Eggers at most describes a single fetch unit which can fetch two or more instructions in a given cycle for decoding by a singe decode unit. This is different from and does not teach or suggest the structure of multiple (e.g. first through fourth) decode units as recited in claim 8. "

However, each instruction MUST be decoded before it can be executed, see page 14, right hand column, line 3. The decoder for the instructions in one of the executing threads is decoded by a first decode unit and the instructions for the other one of the executing threads is decoded by a second decode unit. The claims do not require that the first and second decode units must be separate, independent, and distinct. Therefore, in Eggers et al, the units that decode the instructions for the two executing threads are first and second decode units. Therefore this argument is moot.

15. On page 10, Applicant argues in essence:

> *"With respect to claim 5, Applicants again note that Eggers does not describe any particular structure for the SMT processor proposed therein. Moreover, Eggers at most describes a single fetch unit which can fetch two or more instructions in a given cycle for decoding by a single decode unit. This is different from and does not teach or suggest the structure of multiple (e.g. first through fourth) instruction fetch units as recited in claim 5."*

However, as discussed above, the fetch unit partitions itself among the two executing threads. The partition of the fetch unit fetching one of the two executing threads is the claimed first fetch unit and the partition of the fetch unit fetching the other of the two executing threads is the claimed second fetch unit. The claims do not require that the first and second fetch units must be separate, independent, and distinct. Therefore, in Eggers et al, the units that fetch the instructions for the two executing threads are the claimed first and second fetch units. Therefore this argument is moot.

16. On page 10, Applicant argues in essence:

"With respect to claim 6, applicants note that the register file mentioned in Eggers appears to have different structure and function as compared to the recited four way register file. Merely changing the size of the register file described in Eggers still does not read on the recited four way register file."

However, a register file can have any number of ways. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the register file of Eggers et al. be any number of ways, including four ways, as it has been held that changing size is not a patentable difference. In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

Any other differences in the structure and function of the register file have not been clearly set forth in the claims. Applicant is again arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

As such any such specific structures or functions of the four way register file are not read into the claims. Therefore this argument is moot.

17. On pages 11 and 12, Applicant argues in essence:

"The cited portion of Eggers, namely page 14, left hand column, describes that during the next instruction fetch cycle, a new instruction may be fetched to replace the now inactive instruction, but Eggers does not teach or suggest switching an active thread with a new thread after detecting a stalling event in the active thread."

Applicant is again arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description

contained in the applicant's specification." In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

In this case, the limitation "switching an active thread with a new thread after detecting a stalling event in the active thread" cannot be read into the claims for the purpose of avoiding the prior art. Therefore this argument is moot.

18. On page 12, Applicant argues in essence:

"Eggers fails to teach or suggest the recited switching said first active thread with a third thread, if the third tread is ready to execute."

However, Eggers et al. have taught fetching from two threads each cycle. The fetch unit fetches what will provide the most benefit. The unit has eight threads and the disclosure has taught that any two of the eight threads can be selected during every cycle. Therefore Eggers et al. have inherently taught switching any thread with any of the other threads, including switching said first active thread with a third thread, if the third tread is ready to execute, as claimed. Therefore this argument is moot.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone numbetr for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER

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